A 15 Watt PEP GaAs PHEMT MMIC Power Amplifier For 3G Wireless Transmitter Applications

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Abstract - **This work describes a wide-bandwidth highly integrated MMIC linear power amplifier implemented with high voltage GaAs PHEMT device technology targeting 3G wireless infrastructure applications. The MMIC amplifier exhibits 34 dB small signal gain, less than 0.5 dB gain variation across the UMTS frequency band centered at 2.14GHz, and a peak-envelope power in excess of 15 W when biased with a 12 volt supply. Under a 64 traffic channel single carrier W-CDMA signal (test model 1, with a 11 dB peak-to-average signal ratio), the amplifier achieves 2W average output power and 17% power added efficiency at an ACPR of -40 dBc. Under a 9-channel single carrier IS-95 forward-link signal, the amplifier achieves 4 W average power at an efficiency of 25% at an ACPR of –38 dBc. The MMIC amplifier is highly integrated consisting of 3-gain stages, input and interstage matching circuits, and output pre-matching - - all contained on the GaAs IC. The use of on-chip pre-matching for the output load line greatly simplifies and reduces off chip component matching elements and their tolerances. To the author's best knowledge, this amplifier represents the highest power and efficiency reported to date for a GaAs PHEMT amplifier realized at this level of integration.**

I Introduction

Infrastructure transmitters for third-generation cellular require power amplifiers, which simultaneously exhibit high output power, linearity, and efficiency to meet the stringent requirements imposed in amplifying multi-channel W-CDMA signals. While the final amplifier stage in these transmitters may produce peak-envelope power in excess of 200 W [1], there is also need for amplifiers meeting similar linearity specifications at lower power levels for use as a driver stages and/or final stages in Pico-cell environments. In this paper, we report on a highly integrated MMIC based amplifier using GaAs PHEMT technology.

II PHEMT Device Technology

The amplifier is designed with Motorola's high voltage GaAs pHEMT technology that features a highly manufacturable and robust 0.6 μm gate length titanium tungsten nitride (TiWNi) gate. The epitaxial structure is double delta-doped InGaAs/AlGaAs grown by molecular beam epitaxy having nominal sheet charge and mobility of $2x10^{12}$ cm^{-2} and 6300 cm^2/Vs at room temperature. Silicon nitride passivation prevents degradation due to moisture and environmental factors. Pulsed I-V measurements suggest the devices exhibit minimal low frequency dispersion thereby allowing a high degree of accuracy in the large signal models used in the circuit design process (described later). The process is fully integrated and provides N+ resistors, MIM capacitors, and spiral inductors with 2 layers of metalization and through vias on substrates down to 1 mil thick on 150 mm wafers. Previous work in developing power amplifiers with discrete unmatched transistors has shown the device technology exhibits excellent linearity with good power efficiency under W-CDMA signals [2].

III CIRCUIT Design & Simulation

The amplifier was designed entirely using simulation tools. Particular emphasis was placed on examining the effects of device size, quiescent bias point, and harmonic source/load terminations to optimize the efficiency/linearity trade-off. In a multi-stage linear power amplifier, the design of each stage becomes intertwined with the others due to interaction of multiple active devices and interstage load lines. These effects are difficult to include in load pull measurements, and therefore, the use of conventional load pull characterization methods to experimentally determine these design parameters was not pursued. Instead, a design methodology based on using a large signal model of the PHEMT device coupled with harmonic balance and behavioral modeling methods was adopted.

A large signal model for a unit sized PHEMT device was first developed by measuring the device's S-parameters over a wide region of its I-V space using on-wafer probe methods. This data along with forward biased cold chip S-parameter measurements were used to determine extrinsic parasitic resistances, inductances, and intrinsic parameters for the large signal model. Model parameters are then

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scaled to represent device peripheries larger than the unit sized cell.

The design process first considered the output gain stage consisting of the device along with input/output matching circuitry (described by the fundamental, 2nd, and higher order harmonics) as illustrated in Fig. 1. Load pull simulations were performed with the goal of optimizing the linearity/power/efficiency trade-off. Harmonic balance simulation predictions of am-am, am-pm, and average supply current (I_{DD}), with an input single tone CW stimulus, were performed as functions of device gate width, quiescent point, and fundamental/harmonic source/load terminations. From this data, behavioral analysis techniques based on envelope transfer functions derived from am-am, am-pm, allowed predicting amplifier performance to a W-CDMA stimulus compliant to the 3GPP standard [3]. This technique allows predicting output power, gain, ACPR), and efficiency of the amplifier when driven with this digitally modulated stimulus.

Results from these simulations suggest an optimal Γ_L of 0.87 @ 179° and device gate width for Q3 of ~ 30 mm. This results in a power gain greater than 10 dB (with an output power greater than 15W). In addition, the device is biased deep in Class A/B at less than 5% IDSS. Further, the second harmonic load termination was found to exhibit a significant effect on linearity & efficiency with an optimal value near a short circuit condition. The effect of higher order harmonic terminations as well as source terminations was investigated as well. The results suggest that while additional performance improvements are possible, the resonant circuitry needed to implement these conditions would significantly add to the size and cost of the die and were thus not pursued.

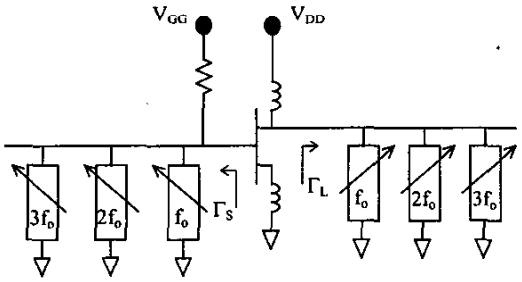

Fig 1 Load pull simulations were performed on the output gain stage as a function of bias and source/load terminations.

The design of the first & second gain stages was accomplished in much the same manner, although more emphasis was placed on achieving linearity, with less focus on efficiency, such that the linearity of the overall amplifier is set primarily by the third gain stage. The bias point of the first two stages was set at a moderate Class A/B level of above 10% IDSS which resulted in a power gain of greater than 10 dB per stage.

The amplifier is designed to be housed in an inexpensive plastic surface mount PFP-16 package as illustrated in Fig. 2. The die is attached to the package flag using soft solder attachment techniques. This package is well suited for moderate power level amplifiers and features a ground plane attachment on the bottom-mating surface for improved electrical and thermal grounding. The package leads exhibit significant length at 2.1 GHz, and therefore, they must be included with the MMIC in forming the input and output matching networks for the amplifier. To this end, a detailed distributed electrical model for the package was utilized and the contributions from these leads were designed as part of the MMIC amplifier's input/output networks.

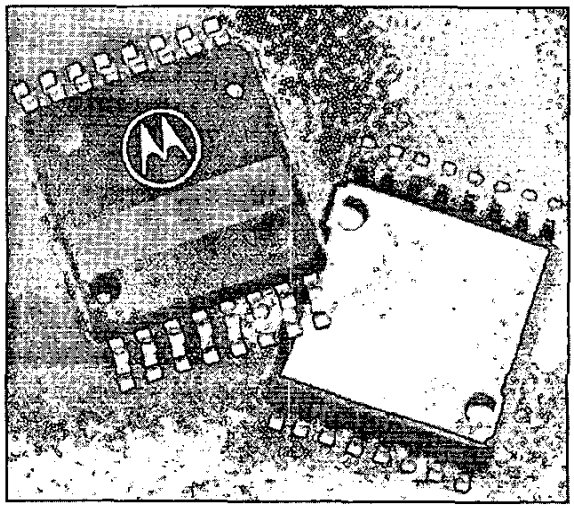

Fig 2 The MMIC amplifier is housed in an inexpensive PFP surface mount package.

A simplified schematic of the three-stage amplifier is depicted in Figure 3. As can be observed, most of the circuitry is contained on a single IC. Some additional decoupling of drain bias lines is realized using high value off-chip capacitors to better terminate baseband frequency components (dc – 5 MHz).

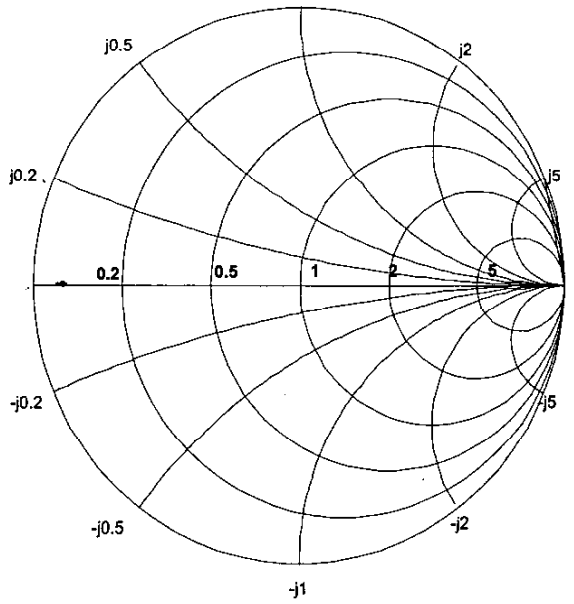

Fig. 4 Measured Q3 load line from 2.0 to 2.4 GHz. Measurements referenced to the drain terminal of Q3.

The Q3 output load line is realized with on-chip pre-matching consisting of series L and shunt C, followed by the package, a short length of off-chip transmission line, and an off-chip shunt C. The use of on-chip pre-matching greatly simplifies and reduces off chip component matching elements and their associated tolerances. This is particularly important in realizing the low impedance required by Q3 and to minimize the tolerance variations and placement of the off chip shunt capacitance. In addition, both Q2 and Q3 load lines are realized with fourth order networks for improved bandwidth performance. This is particularly important for minimizing gain variations with frequency. The PFP-16 package leads form an integral part of the matching structure. Their electrical contributions are effectively embedded into both input and output networks. An on-chip second harmonic termination is included on the GaAs die in conjunction with output transistor Q3.

Measurements were made to determine the effectiveness of the output line network topology. Measurements made on circuits where the S-parameters are referenced to the Q3 drain terminals are shown in Figure 4. As illustrated, a reflection coefficient of near 0.87 @ 179° is maintained over a very broad bandwidth.

IV MEASURED Results

Measured power performance with the GaAs MMIC amplifier housed in a plastic PFP-16 package are illustrated in Fig 5 under a pulsed single tone CW stimulus. At 1 dB gain compression, better than 15W of output power is achieved. Performance under 64 channel W-CDMA (test model 1) and a 9 channel forward link IS-95 CDMA stimulus are illustrated in Figs. 6a and 6b, respectively (f_o=2.14 GHz). The amplifier achieves 2W output power and 17% efficiency at an ACPR of –40 dBc for the multi-channel W-CDMA stimulus. Under power back-off conditions, the ACPR drops to near –50 dBc indicating low am-am and am-pm distortion at lower drive levels. For the 9 channel IS-95 signal, 4W of output power and 25% power added efficiency are achieved at a linearity of –38 dBc. Power gain for both signal formats is 33 dB and the drain bias voltage is 12 volts. Gain variation is minimized to 0.5 dB from 2.1 to 2.2 GHz. Input and output return loss is better than 10 dB.

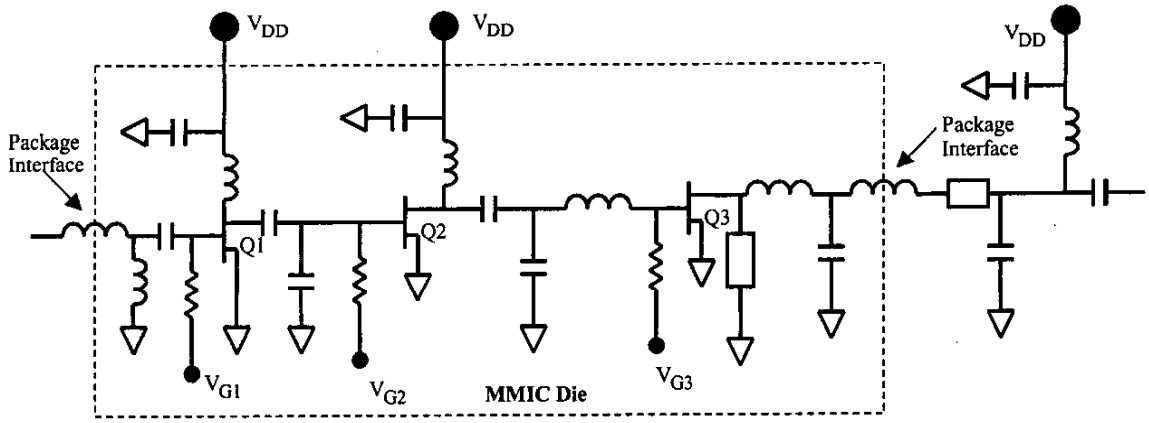

Fig. 3 Simplified schematic of power amplifier

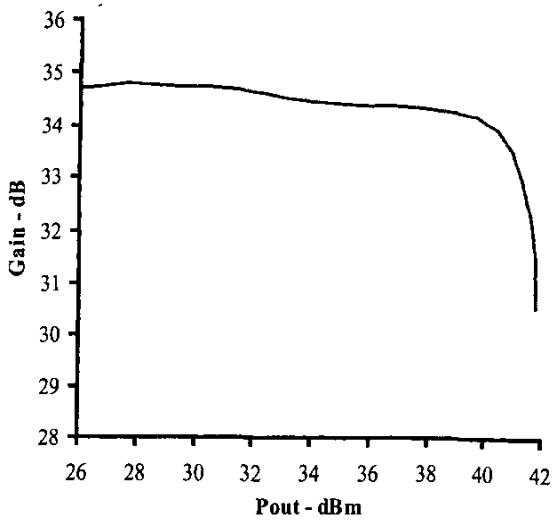

Fig. 5 Measured amplifier performance under CW pulsed conditions with VDD=12 volts.

V Summary

A high efficiency state-of-the-art GaAs PHEMT MMIC amplifier has been designed and fabricated. Housed in an inexpensive PFP plastic package, the amplifier achieves 15W-peak envelope power. Under CDMA modulated drive, the amplifier achieves excellent efficiency with good linearity. The design incorporates on-chip pre-matching for the output load line, which greatly simplifies the number of off-chip components and eases their component tolerances and placement significantly improving manufacturablility.

VI References:

[1] I. Takenaka, *et al.*, "A 240 W Power Heterojunction FET with High Efficiency for W-CDMA Base Stations", IEEE International Microwave Symposium, Phoenix, AZ, June, 2000

[2] M. Miller, *et al.*, "A Power PHEMT Device Technology for Broadband Wireless Access", IEEE International Microwave Symposium, Phoenix, AZ, June, 20003

[3] 3rd Generation Partnership Project, Technical Specifications Group Radio Access Networks, Base Station Conformance Specification: Radio Transmission and Reception (FDD), Release 99.3G TS25.141.

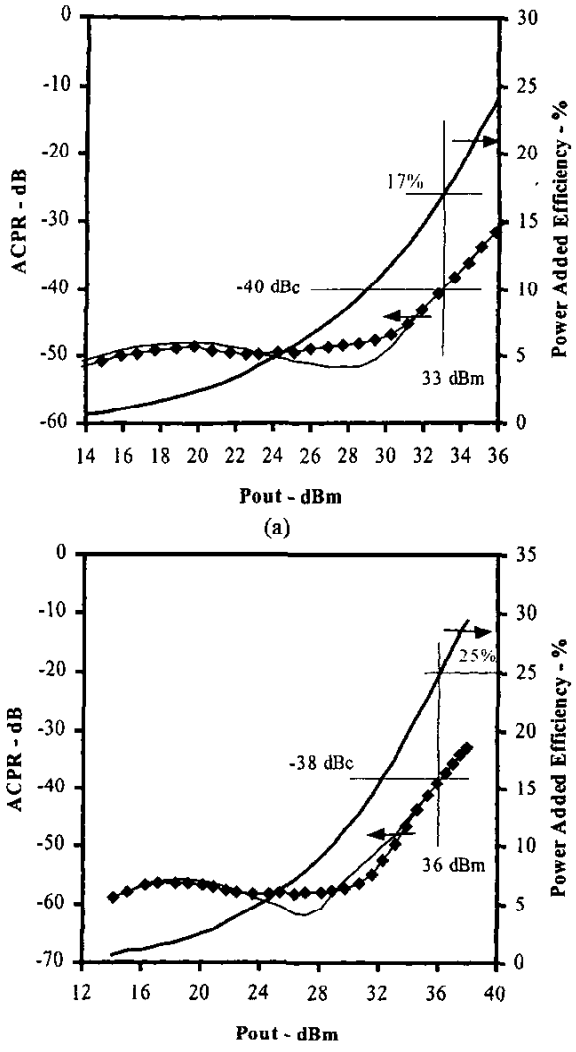

Fig. 6 Measured amplifier performance with a CDMA stimulus. a) 64 channel W-CDMA single carrier per test model 1, and b) 9 channel IS-95 forward link signal.